AMENDMENT TO THE CLAIMS

Claim 1-20 Canceled

21. (original) An electrically programmable memory element, comprising:

a first dielectric layer;

a first conductive layer formed over said first dielectric layer;

a second dielectric layer formed over said first conductive layer, said second dielectric layer having an opening therethrough to said first conductive layer;

a spacer disposed about a peripheral portion of said opening to form a pore;

a programmable resistance material disposed within said pore; and

a second conductive layer formed over said programmable resistance material.

22. (original) The memory element of claim 21, wherein said spacer is formed by the method comprising the steps of:

forming a third dielectric layer over a peripheral portion of of said opening; and

removing a portion of said third dielectric layer.

23. (original) The memory element of claim 21, further comprising:

a third conductive layer electrically coupled between said first conductive layer and a substrate, wherein substantially all electrical communication between said second conductive layer and said first conductive layer is through an edge portion of said third conductive layer.

24. (original) The memory element of claim 23, wherein said third conductive layer comprises a sidewall layer.

25. (original) The memory element of claim 23, wherein said third conductive layer is a conductive sidewall spacer or a conductive sidewall liner.

26. (original) The memory element of claim 21, wherein said programmable resistance material comprises a phase change material.

27. (original) The memory element of claim 21, wherein said programmable resistance material comprises a chalcogen element.

Claim 28-59 Canceled

60. (new) The memory element of claim 28, wherein at least a portion of said first dielectric layer is underlying said pore.